Page 37, line 3, delete "is held" and insert -- holds --;
line 18, delete "more" and insert --further --.

IN THE CLAIMS:

Please cancel claims 1-6 without prejudice or disclaimer of the matter therein.

Please add new claims 7-125 as follows:

-- 7. A semiconductor integrated circuit comprising:

a first circuit supplied with an external supply voltage, which outputs a voltage whose amplitude has small dependence on an amplitude of the external supply voltage when the external supply voltage is larger than a predetermined voltage;

a second circuit, supplied with the external supply voltage, which outputs a voltage whose amplitude has large dependence on an amplitude of the external supply voltage; and

an internal circuit supplied with the output voltage of said first circuit;

wherein the output of said second circuit is coupled to the output of said first circuit.

8. The semiconductor integrated circuit according to claim 7, wherein said first circuit includes a first MOS transistor whose drain is coupled to the output of said first circuit, and

wherein said first circuit has a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

9. The semiconductor integrated circuit according to claim 7, wherein said second circuit includes a second MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit.

10. The semiconductor integrated circuit according to claim 8, wherein said second circuit includes a second MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit.

11. The semiconductor integrated circuit according to claim 7, wherein said second circuit supplies the output voltage thereof during aging test.

12. The semiconductor integrated circuit according to claim 8, wherein said second circuit supplies the output voltage thereof during aging test.

13. The semiconductor integrated circuit according to claim 9, wherein said second circuit supplies the output voltage thereof during aging test.

14. The semiconductor integrated circuit according to claim 10, wherein said second circuit supplies the output voltage thereof during aging test.

15. A semiconductor integrated circuit comprising:

a first circuit, supplied with an external supply voltage, which outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes in a level larger than predetermined voltage;

a second circuit, supplied with the external supply voltage, which outputs a voltage changing at a second rate which is larger than the first rate; and

an internal circuit supplied with the output voltage of said first circuit;

wherein the output of said second circuit is coupled to the output of said first circuit.

16. The semiconductor integrated circuit according to claim 15, wherein said first circuit includes a first MOS transistor whose drain is coupled to the output of said first circuit, and

wherein said first circuit has a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

17. The semiconductor integrated circuit according to claim 15, wherein said second circuit includes a second MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit.

18. The semiconductor integrated circuit according to claim 16, wherein said second circuit includes a second MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit.

19. The semiconductor integrated circuit according to claim 15, wherein said second circuit supplies the output voltage thereof during aging test.

20. The semiconductor integrated circuit according to claim 16, wherein said second circuit supplies the output voltage thereof during aging test.

21. The semiconductor integrated circuit according to claim 17, wherein said second circuit supplies the output voltage thereof during aging test.

22. The semiconductor integrated circuit according to claim 18, wherein said second circuit supplies the output voltage thereof during aging test.

23. A semiconductor integrated circuit comprising:

a first circuit, supplied with an external supply voltage, which outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes in a level larger than predetermined voltage;

an internal circuit supplied with the output voltage of said first circuit; and

a second circuit having a MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit;

wherein the MOS transistor is turned on when said internal circuit needs a larger voltage than the voltage changing at the first rate.

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24. The semiconductor integrated circuit according to claim 23, wherein said first circuit includes a first MOS transistor whose drain is coupled to the output of said first circuit, and

wherein said first circuit has a feed back circuit between the gate of said first MOS transistor and the output of said first circuit.

25. The semiconductor integrated circuit according to claim 23, wherein the MOS transistor of said second circuit is turned on during aging test.

26. The semiconductor integrated circuit according to claim 24, wherein the MOS transistor of said second circuit is turned on during aging test.

27. A semiconductor integrated circuit comprising:

a first circuit, supplied with an external supply voltage, which outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes in a level larger than predetermined voltage;

an internal circuit supplied with the output voltage of said first circuit; and

a second circuit having a MOS transistor whose source-drain path is coupled between the external supply voltage and the output of said first circuit;

wherein the MOS transistor is turned on to provide a larger voltage than the voltage changing at the first rate.

28. The semiconductor integrated circuit according to claim 27, wherein said first circuit includes a first MOS transistor whose drain is coupled to the output of said first circuit, and

wherein said first circuit has a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

29. The semiconductor integrated circuit according to claim 27, wherein the MOS transistor of said second circuit is turned on during aging test.

30. The semiconductor integrated circuit according to claim 28, wherein the MOS transistor of said second circuit is turned on during aging test.

31. The semiconductor integrated circuit according to claim 7, wherein the amplitude of the output voltage of said first circuit is to enable aging test by enlarging the amplitude of the external supply voltage.

32. The semiconductor integrated circuit according to claim 7, further comprising:

a third circuit which outputs a voltage whose amplitude has small dependence on an amplitude of the external supply voltage when the external supply voltage is larger than predetermined voltage.

33. The semiconductor integrated circuit according to claim 7, further comprising:

a fourth circuit operated by supplied with the external supply voltage, which transfers a signal to said internal circuit.

34. The semiconductor integrated circuit according to claim 33, further comprising:

a back bias generator supplying a back bias voltage to a region of a silicon substrate of the semiconductor integrated circuit.

35. The semiconductor integrated circuit according to claim 33, wherein said fourth circuit has a larger device than that of said internal circuit.

36. The semiconductor integrated circuit according to the claim 35, wherein said larger device of said fourth circuit is a MOS transistor which has a larger thickness of a gate insulator than that of a MOS transistor of said internal circuit.

37. The semiconductor integrated circuit according to claim 35, wherein said larger device of said fourth circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

38. The semiconductor integrated circuit according to claim 7, wherein said predetermined voltage is determined by a voltage reference.

39. The semiconductor integrated circuit according to claim 38, wherein said voltage reference is determined by using a threshold voltage of a first MOS transistor.

40. The semiconductor integrated circuit according to claim 7, wherein a load capacitance of said internal circuit changes in accordance with a signal.

41. The semiconductor integrated circuit according to claim 15, wherein the amplitude of the output voltage of said first circuit enables aging test by enlarging the amplitude of the external supply voltage.

42. The semiconductor integrated circuit according to claim 15, wherein said second circuit makes the changing rate of the output voltage of said first circuit larger during aging test.

43. The semiconductor integrated circuit according to claim 15, further comprising:

a third circuit, supplied with the external supply voltage, which transfers a signal to said internal circuit.

44. The semiconductor integrated circuit according to claim 43, further comprising:

a back bias generator supplying a back bias voltage to a region of a silicon substrate of the semiconductor integrated circuit.

45. The semiconductor integrated circuit according to claim 43, wherein said third circuit has a larger device than that of said internal circuit.

46. The semiconductor integrated circuit according to claim 45, wherein said larger device of said third circuit is a MOS transistor which has a larger thickness of a gate insulator than that of a MOS transistor of said internal circuit.

47. The semiconductor integrated circuit according to claim 45, wherein said larger device of said third circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

48. The semiconductor integrated circuit according to claim 15, wherein said predetermined voltage is determined by a voltage reference.

49. The semiconductor integrated circuit according to claim 48, wherein said voltage reference is determined by using a threshold voltage of a MOS transistor.

50. The semiconductor integrated circuit according to claim 15, wherein a load capacitance of said internal circuit changes in accordance with a signal.

51. The semiconductor integrated circuit according to claim 23, wherein the amplitude of the output voltage of said first circuit is to enables aging test by enlarging the amplitude of the external supply voltage.

52. The semiconductor integrated circuit according to claim 23, further comprising:

a third circuit, supplied with the external supply voltage, which transfers a signal to said internal circuit.

53. The semiconductor integrated circuit according to claim 52, further comprising:

a back bias generator supplying a back bias voltage to a region of a silicon substrate of the semiconductor integrated circuit.

54. The semiconductor integrated circuit according to claim 52, wherein said third circuit has a larger device than that of said internal circuit.

55. The semiconductor integrated circuit according to claim 54, wherein said larger device of said third circuit is a MOS transistor which has a larger thickness of the gate

insulator than that of a MOS transistor of said internal circuit.

56. The semiconductor integrated circuit according to claim 54, wherein said larger device of said third circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

57. The semiconductor integrated circuit according to claim 23, wherein said predetermined voltage is determined by a voltage reference.

58. The semiconductor integrated circuit according to claim 57, wherein said voltage reference is determined by using threshold voltage of said first MOS transistor.

59. The semiconductor integrated circuit according to claim 23, wherein a load capacitance of said internal circuit changes in accordance with a signal.

60. The semiconductor integrated circuit according to claim 27, wherein the amplitude of the output voltage of said first circuit enables aging test by enlarging the amplitude of the external supply voltage.

61. The semiconductor integrated circuit according to claim 27, wherein said second circuit makes the changing rate

of the output voltage of said first circuit larger during aging test.

62. The semiconductor integrated circuit according to claim 27, further comprising:

a third circuit, supplied with the external supply voltage, which transfers a signal to said internal circuit.

63. The semiconductor integrated circuit according to claim 62, further comprising:

a back bias generator supplying a back bias voltage to a region of the silicon substrate of the semiconductor integrated circuit.

64. The semiconductor integrated circuit according to claim 62, wherein said third circuit has a larger device than that of said internal circuit.

65. The semiconductor integrated circuit according to claim 64, wherein said larger device of said third circuit is a MOS transistor which has a larger thickness of a gate insulator than that of a MOS transistor of said internal circuit.

66. The semiconductor integrated circuit according to claim 64, wherein said larger device of said third circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

67. The semiconductor integrated circuit according to claim 27, wherein said predetermined voltage is determined by a voltage reference.

68. The semiconductor integrated circuit according to claim 67, wherein said voltage reference is determined by using a threshold voltage of a MOS transistor.

69. The semiconductor integrated circuit according to claim 27, wherein a load capacitance of said internal circuit changes in accordance with a signal.

70. A semiconductor integrated circuit comprising:

a first circuit, supplied with an external supply voltage, which outputs a voltage whose amplitude has small dependence on an amplitude of the external supply voltage when the external supply voltage is larger than predetermined voltage;

a second circuit coupled to said first circuit; and

an internal circuit supplied with the output voltage of said first circuit;

wherein said second circuit makes the amplitude of the output voltage of said first circuit when the external supply voltage is larger than predetermined voltage to be larger.

71. The semiconductor integrated circuit according to claim 70, wherein said first circuit includes a first MOS transistor having a source-drain path with which said internal circuit makes a current path, and

wherein the output of said second circuit is coupled to the gate of said first MOS transistor.

72. The semiconductor integrated circuit according to claim 70, wherein the amplitude of the output voltage of said first circuit enables aging test by enlarging the amplitude of the external supply voltage.

73. The semiconductor integrated circuit according to claim 70, wherein said second circuit makes the dependence of the amplitude of the output voltage of said first circuit larger during aging test.

74. The semiconductor integrated circuit according to claim 70, further comprising:

a third circuit which outputs a voltage whose amplitude has small dependence on an amplitude of the external supply voltage when the external supply voltage is larger than predetermined voltage.

75. The semiconductor integrated circuit according to claim 70, further comprising:

a fourth circuit, supplied with the external supply voltage, which transfers a signal to said internal circuit.

76. The semiconductor integrated circuit according to claim 75, further comprising:

a back bias generator supplying a back bias voltage to a region of a silicon substrate of the semiconductor integrated circuit.

77. The semiconductor integrated circuit according to claim 75, wherein said fourth circuit has a larger device than that of said internal circuit.

78. The semiconductor integrated circuit according to claim 77, wherein said larger device of said fourth circuit is a MOS transistor which has a larger thickness of a gate insulator than that of a MOS transistor of said internal circuit.

79. The semiconductor integrated circuit according to claim 77, wherein said larger device of said fourth circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

80. The semiconductor integrated circuit according to claim 70, wherein said predetermined voltage is determined by a voltage reference.

81. The semiconductor integrated circuit according to claim 80, wherein said voltage reference is determined by using a threshold voltage of a MOS transistor.

82. The semiconductor integrated circuit according to claim 70, wherein said first circuit has a first MOS transistor having a source-drain path with which said internal circuit makes a current path, and a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

83. The semiconductor integrated circuit according to claim 70, wherein a load capacitance of said internal circuit changes in accordance with a signal.

84. The semiconductor integrated circuit according to claim 70, wherein the output of said second circuit is coupled to the output of said first circuit.

85. A semiconductor integrated circuit comprising:

a first circuit, supplied with an external supply voltage, which outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes in a level larger than predetermined voltage;

a second circuit coupled to said first circuit; and

an internal circuit supplied with the output voltage of said first circuit;

wherein said second circuit makes the changing rate of the output voltage of said first circuit larger.

86. The semiconductor integrated circuit according to claim 85, wherein said first circuit includes a first MOS transistor having a source-drain path with which said internal circuit makes a current path, and

wherein the output of said second circuit is coupled to the gate of said first MOS transistor.

87. The semiconductor integrated circuit according to claim 85, wherein the amplitude of the output voltage of said first circuit enables aging test by enlarging the amplitude of the external supply voltage.

88. The semiconductor integrated circuit according to claim 85, wherein said second circuit makes the changing rate of the output voltage of said first circuit larger during aging test.

89. The semiconductor integrated circuit according to claim 85, further comprising:

a third circuit which outputs a voltage whose amplitude has small dependence on an amplitude of the external

supply voltage when the external supply voltage is larger than predetermined voltage.

90. The semiconductor integrated circuit according to claim 85, further comprising:

a fourth circuit, supplied with the external supply voltage, which transfers a signal to said internal circuit.

91. The semiconductor integrated circuit according to claim 90, further comprising:

a back bias generator supplying a back bias voltage to a region of a silicon substrate of the semiconductor integrated circuit.

92. The semiconductor integrated circuit according to claim 90, wherein said fourth circuit has a larger device than that of said internal circuit.

93. The semiconductor integrated circuit according to claim 92, wherein said larger device of said fourth circuit is a MOS transistor which has a larger thickness of a gate insulator than that of a MOS transistor of said internal circuit.

94. The semiconductor integrated circuit according to claim 92, wherein said larger device of said fourth circuit is

a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

95. The semiconductor integrated circuit according to claim 85, wherein said predetermined voltage is determined by a voltage reference.

96. The semiconductor integrated circuit according to claim 95, wherein said voltage reference is determined by using a threshold voltage of a MOS transistor.

97. The semiconductor integrated circuit according to claim 85, wherein said first circuit has a first MOS transistor having a source-drain path with which said internal circuit makes a current path, and a feedback circuit between the gate of said first MOS transistor and the output of said first circuit.

98. The semiconductor integrated circuit according to claim 85, wherein a load capacitance of said internal circuit changes in accordance with a signal.

99. The semiconductor integrated circuit according to claim 85, wherein the output of said second circuit is coupled to the output of said first circuit.

100. A semiconductor integrated circuit comprising:

a first circuit, supplied with an external supply voltage, which outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes in a level larger than predetermined voltage;

an internal circuit supplied with the output voltage of said first circuit; and

a second circuit having a first MOS transistor whose source-drain path is coupled between the external supply voltage and said first circuit;

wherein the first MOS transistor is turned on when said internal circuit needs a larger voltage than the voltage changing at the first rate.

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101. The semiconductor integrated circuit according to claim 100, wherein said first circuit includes a second MOS transistor having a source-drain path with which said internal circuit makes a current path, and

wherein the output of said second circuit is coupled to the gate of said second MOS transistor.

102. The semiconductor integrated circuit according to claim 100, wherein the first MOS transistor is turned on during aging test.

103. The semiconductor integrated circuit according to claim 100, further comprising:

a third circuit, supplied with the external supply voltage, which transfers a signal to said internal circuit.

104. The semiconductor integrated circuit according to claim 103, further comprising:

a back bias generator supplying a back bias voltage to a region of the silicon substrate of the semiconductor integrated circuit.

105. The semiconductor integrated circuit according to claim 103, wherein said third circuit has a larger device than that of said internal circuit.

106. The semiconductor integrated circuit according to claim 105, wherein said larger device of said third circuit is a MOS transistor which has a larger thickness of the gate insulator than that of a MOS transistor of said internal circuit.

107. The semiconductor integrated circuit according to claim 105, wherein said larger device of said third circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

108. The semiconductor integrated circuit according to claim 100, wherein said predetermined voltage is determined by a voltage reference.

109. The semiconductor integrated circuit according to claim 108, wherein said voltage reference is determined by using a threshold voltage of a MOS transistor.

110. The semiconductor integrated circuit according to claim 100, wherein said first circuit has a second MOS transistor having a source-drain path with which said internal circuit makes a current path, and a feedback circuit between the gate of said second MOS transistor and the output of said first circuit.

111. The semiconductor integrated circuit according to claim 100, wherein a load capacitance of said internal circuit changes in accordance with a signal.

112. The semiconductor integrated circuit according to claim 100, wherein the output of said second circuit is coupled to the output of said first circuit.

113. A semiconductor integrated circuit comprising:

a first circuit, supplied with an external supply voltage, which outputs a voltage changing at a first rate which is smaller than the changing rate of the external supply voltage, when the external supply voltage changes in a level larger than predetermined voltage;

an internal circuit supplied with the output voltage of said first circuit; and

a second circuit having a first MOS transistor whose source-drain path is coupled between the external supply voltage and said first circuit;

wherein the first MOS transistor is turned on so that said first circuit can provide a larger voltage than the voltage changing at the first rate.

114. The semiconductor integrated circuit according to claim 113, wherein said first circuit includes a second MOS transistor having a source-drain path with which said internal circuit makes a current path, and

wherein the output of said second circuit is coupled to the gate of said second MOS transistor.

115. The semiconductor integrated circuit according to claim 113, wherein the first MOS transistor is turned on during aging test.

116. The semiconductor integrated circuit according to claim 113, further comprising:

a third circuit, supplied with the external supply voltage, which transfers a signal to said internal circuit.

117. The semiconductor integrated circuit according to claim 116, further comprising:

a back bias generator supplying a back bias voltage to a region of the silicon substrate of the semiconductor integrated circuit.

118. The semiconductor integrated circuit according to claim 116, wherein said third circuit has a larger device than that of said internal circuit.

119. The semiconductor integrated circuit according to claim 118, wherein said larger device of said third circuit is a MOS transistor which has a larger thickness of a gate insulator than that of a MOS transistor of said internal circuit.

120. The semiconductor integrated circuit according to claim 118, wherein said larger device of said third circuit is a MOS transistor which has a longer gate length than that of a MOS transistor of said internal circuit.

121. The semiconductor integrated circuit according to claim 113, wherein said predetermined voltage is determined by a voltage reference.

122. The semiconductor integrated circuit according to claim 121, wherein said voltage reference is determined by using a threshold voltage of a MOS transistor.